Abstracts

Optimum Design of Distributed Power-FET Amplifiers -- Application to a 2 - 18 GHz MMIC Module Exhibiting Improved Power Performances

M. Campovecchio, B. Le Bras, M. Lajugie and J. Obregon. "Optimum Design of Distributed Power-FET Amplifiers -- Application to a 2 - 18 GHz MMIC Module Exhibiting Improved Power Performances." 1994 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest 94.1 (1994 [MCS]): 125-128.

A suitable and effective design method of distributed power amplifiers, based on the optimum FET load requirement for power operation, is proposed in this paper. An analytical determination of the gate and drain line characteristic admittances provides both the initial values and right directions for an optimum design. The best trade-offs between wide band and high power operation have been investigated. To validate the method, a FET amplifier demonstrator with a gate periphery of 1.2 mm has been manufactured at the Texas Instruments foundry. The MMIC amplifier demonstrated state of the art power density performance of 340 mW/mm over the 2-18 GHz band associated with 14.2% power added efficiency, 26.5 % drain efficiency and 26.1 dBm output power at 1 dB compression in CW operation.

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